**BİLGİSAYAR ORGANİZASYONU VE TASARIMI LABORATUVARI UYGULAMA RAPORU**

**UYGULAMA NO:** 3

**UYGULAMA TARİHİ:** 30 KASIM 2016

**GRUP NO:**  G8

**GRUP ÜYELERİ**

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**Bölüm 1**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

ENTITY flipflop IS

PORT ( D, Clock : IN STD\_LOGIC ;

Q : INOUT STD\_LOGIC;

Qx : INOUT STD\_LOGIC) ;

END flipflop ;

ARCHITECTURE Behavior OF flipflop IS

BEGIN

PROCESS ( Clock )

BEGIN

IF Clock'EVENT AND Clock = '1' THEN

Q <= D ;

Qx <= NOT D;

END IF ;

END PROCESS ;

END Behavior ;

LIBRARY ieee ;

USE ieee.std\_logic\_1164.all ;

entity devre is

Port ( x : in STD\_LOGIC;

saat : in STD\_LOGIC;

z : out STD\_LOGIC);

end devre;

architecture STRUCTURAL of devre is

component flipflop is PORT ( D, Clock : IN STD\_LOGIC ;

Q : INOUT STD\_LOGIC;

Qx : INOUT STD\_LOGIC); end component;

signal D1,Q1,Q1x,D2,Q2,Q2x :std\_logic;

begin

D1<= Q1x OR Q2;

D2<= X AND Q2x;

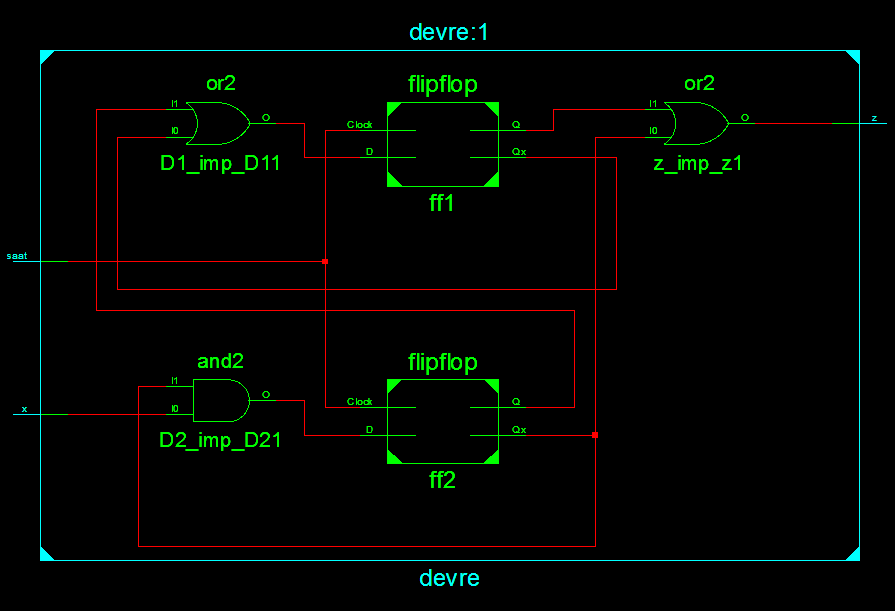
ff1 : flipflop port map(D1,saat,Q1,Q1x);

ff2 : flipflop port map(D2,saat,Q2,Q2x);

Z<= Q2x OR Q1;

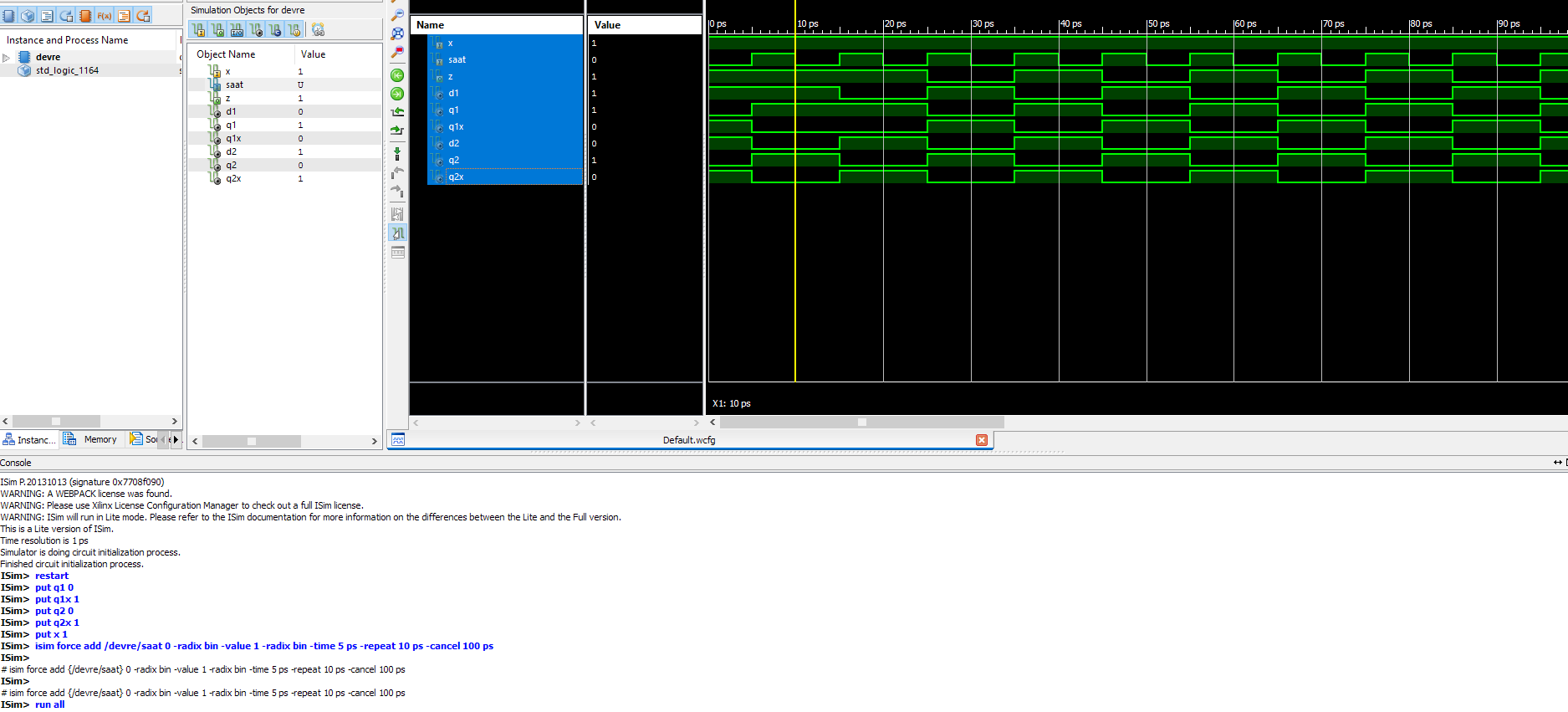
end structural;

**Bölüm 2**



RTL şeması

**Bölüm 3**



Waveform Diagram